A Novel Control Method to Minimize Distortion in AC Inverters

Dennis Gyma

Hewlett-Packard Company
150 Green Pond Road
Rockaway, NJ 07866

ABSTRACT

In PWM AC inverters, the duty-cycle modulator transfer function must be highly linear to achieve low distortion. Current-mode (CM) control, inherently non-linear, is needed to actively "damp" otherwise high-Q LC noise-reduction filters. A novel current-mode control approach is proposed which tailors external ramp characteristics to achieve "perfect" transfer function linearity regardless of duty cycle, and guarantee sub-harmonic stability. Supporting mathematical analysis and prototype measurements are included.

The method when applied to DC/DC converters provides fixed gain-bandwidth in the continuous conduction mode over a broad line and load range.

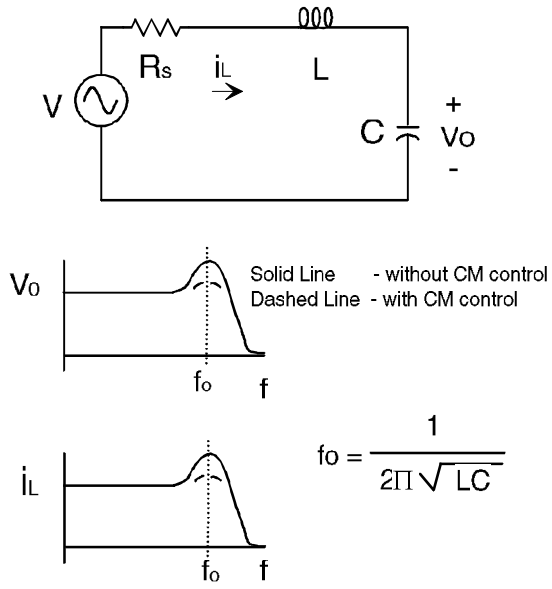
I. INTRODUCTION

The overall goal of the work is to design a low-distortion, low-noise switching DC/AC inverter. The paper will demonstrate that achieving low distortion requires a linear transfer function for the duty-cycle modulator (PWM) function.

To meet the output noise specifications, a low-pass, LC output filter is required to attenuate switching frequency noise components to an acceptable level. The filter values are chosen to yield the desired noise attenuation, output impedance, and to keep inverter rms current stresses to acceptable levels. The resulting high-Q LC filter exhibits resonant peaking of approximately 20dB in the filter transfer function as shown in Figure 1.

This peaking severely limits bandwidth when trying to regulate output voltage, since the filter transfer function appears in the open-loop gain of the output voltage control loop. Lower bandwidth results in poorer performance: lower frequency response, greater distortion, and higher output impedance. Passively damping the high-Q filter is

Figure 1- Output Noise Attenuation Filter



impractical, since it would lower the efficiency to the equivalent of linear audio amplifier technology. Therefore, the well-known technique of current-mode control was used to actively "damp" the output filter. Current-mode control virtually eliminates the LC resonance, by actively regulating the current, and therefore eliminating the peaking in current and therefore output voltage at the LC resonant frequency. The voltage control loop bandwidth can now be increased to improve the previously mentioned performance characteristics. Figure 1 shows the filter transfer function with and without the current-mode control loop. Though using current-mode control allows for improved bandwidth, it creates another problem. Current mode control relies on using the inductor current as the timing ramp for the duty-cycle modulator. It will be shown below that the slope of this ramp is operating point or duty-cycle dependent, so the modulator transfer function becomes non-linear over its operating range. This non-linearity creates unwanted distortion components.

Figure 2- Full Bridge Inverter

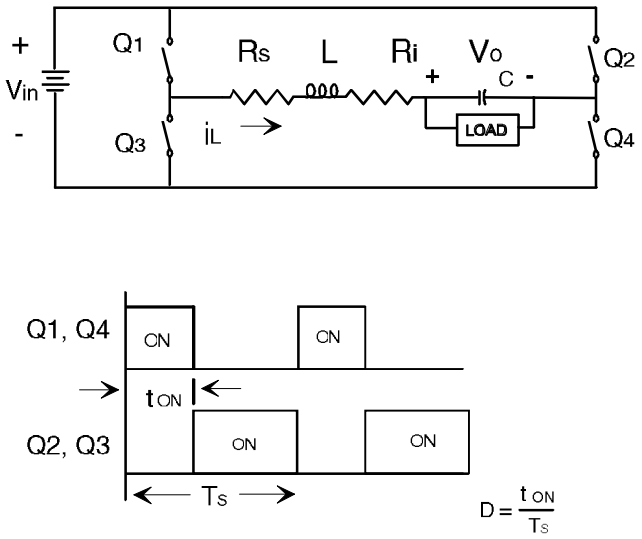
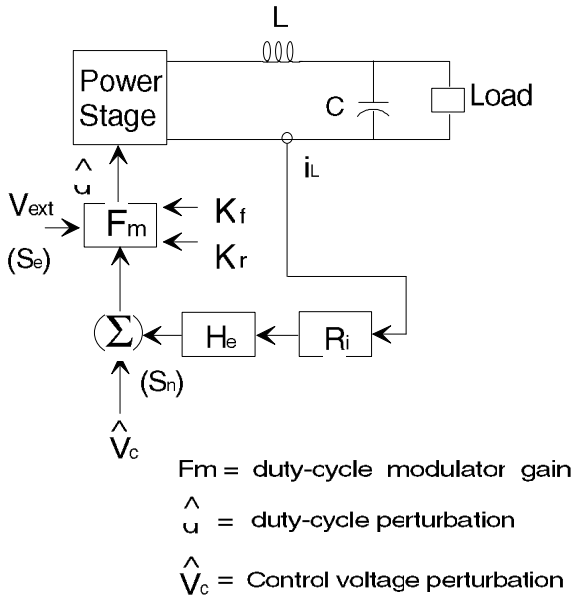


Figure 3- Ridley Current-Mode Control Model



A. Variation in Duty-Cycle Modulator Gain

A full-bridge inverter is shown in Figure 2. The switch pair Q1, Q4 is driven on (conducts) during t_{on} and switch pair Q2, Q3 is held off. For the remainder of the cycle, switch pair Q2, Q3 is on, and switch pair Q1, Q4 is off. The duty cycle is given as $D = t_{on}/T_s$. The expression for the output voltage for the full bridge inverter is derived by equating the inductor volt-seconds during both portions of the switching cycle, and is

$$(V_{in} - V_o)D = (V_{in} + V_o)(1 - D)$$

$$V_o = V_{in}(2D - 1) \qquad (1)$$

Note that V_o is linearly proportional to duty-cycle for this inverter. The inductor current is sensed by resistor R_i (Figure 2), producing a modulator timing ramp whose slope is

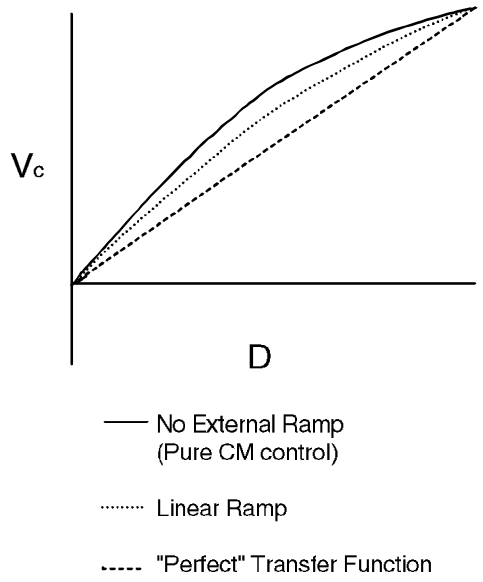
$$s_n = (V_{in} - V_o)R_i/L = 2V_{in}(1 - D)R_i/\mathrm{L} \qquad (2)$$

where D is the duty cycle. From the small signal[1] current-mode control model (Figure 3), we know that the modulator gain is

$$F_m = d/V_c = 1/(s_n + s_e)T_s \qquad (3)$$

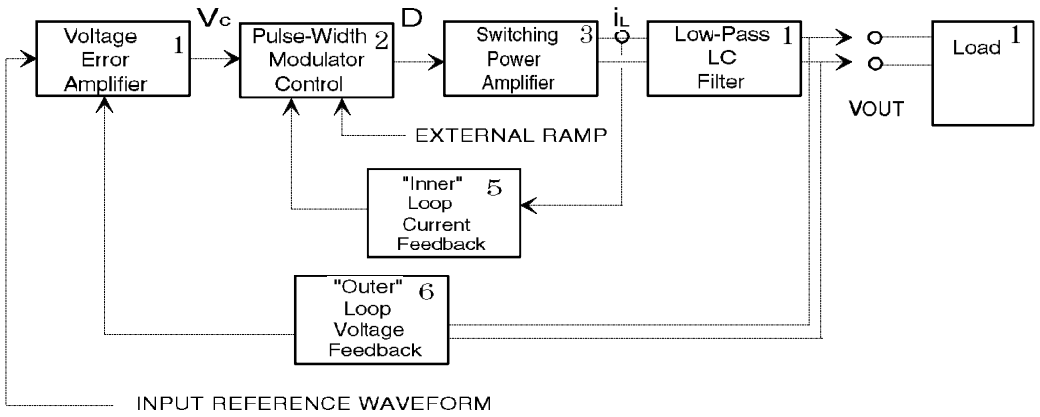
where s_n is the inductor current slope measured through

Figure 4- Modulator Transfer Function



R_i , s_e is an external independent timing ramp added to eliminate sub-harmonic instability, and T_s is the switching period. Since s_n varies with duty cycle, and s_e is generally chosen to be a fixed slope (linear) ramp, Fm therefore varies with duty cycle. This results in a non-linear output (since $V_o \propto D$) for a linear input variation in the modulator control input, V_c. The modulator transfer function, duty-cycle (D) vs V_c , is plotted for pure CM control, CM control with the

Figure 5- Inverter Control Loop Block Diagram



addition of a linear external ramp s_e, along with the "perfect" transfer function we desire in Figure 4. Note that adding more linear ramp reduces, but does not completely eliminate the non-linearity. The expression for the transfer function (D vs V_c) is derived in the next section.

Referring to the block diagram shown in Figure 5, the outer voltage loop has to have enough gain at the frequencies of interest to preserve the desired waveshape. At higher output frequencies, the open-loop gain of the outer loop is decreasing, since it has finite gain-bandwidth, making it less able to reject or attenuate unwanted distortion components.

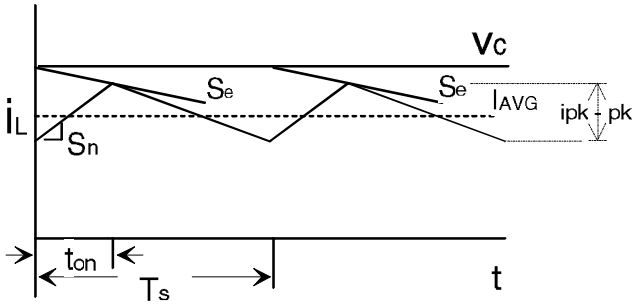
B. Modifying the External Ramp Characteristic to Linearize the Modulator

The inductor current waveform must be examined to gain an understanding of large signal behavior over the operating range of the modulator. Figure 6 is a sketch of the inductor current, i_L, voltage ramp, s_e, and control voltage, V_c . Figure 7 illustrates how these signals sum at the PWM comparator input. The switch point to end the on-time(t_{on}) occurs when these signals sum to zero. For this analysis, the filter capacitance chosen (C in Figure 1) is large enough that the capacitor voltage ripple is small, and the inductor current can therefore be assumed to be a linear ramp. Equation (4) describes the relationship between control voltage, V_c, average inductor current, i_{avg}, inductor current ripple, i_{pk-pk} , and external ramp, V_{ext} , as

$$V_c = i_{avg}R_i + (i_{pk-pk})R_i/2 + V_{ext} \quad (4)$$

For the full-bridge inverter (Figure 2), the expression for i_{pk-pk} is

Figure 6- Inductor Current, Vc, Se



$$i_{pk-pk} = 2V_{in}T_s(1-D)D/L \quad (5)$$

Combining (4) and (5) gives

$$V_c = i_{avg}R_i + (V_{in}R_iT_s/L)(D - D^2) + V_{ext} \quad (6)$$

We see from the first term in (6) that i_{avg} is linearly proportional to V_c. However the second term contains a square term, which needs to be eliminated to linearize the relationship between D and V_c . With $i_{avg} = 0$ for the no-load condition to simplify analysis, the expression for V_{ext} that results in V_c being linearly proportional to D is determined.

Setting $V_c = KD$

$$V_c = KD = (V_{in}R_iT_s/L)(D - D^2) + V_{ext} \quad (7)$$

To eliminate the D^2 term

$$V_{ext} = (V_{in}R_iT_s/L)D^2 \quad (8)$$

which then yields

$$V_c = KD = (V_{in}R_iT_s/L)D \quad (9)$$

where $K = V_{in}R_iT_s/L$

The modulator gain, Fm, can now be determined as

$$F_m = 1/(s_n + s_e)T_s \quad (10)$$

$$s_n = 2V_{in}R_i(1 - D)/L \quad (11)$$

Differentiating (8) gives

$$s_e = \frac{d}{dt}(V_{ext}) = 2(V_{in}R_iT_s/L)D(1/T_s) \quad (12)$$

Combining (2) and (12) yields

$$s_n + s_e = 2V_{in}R_i(1 - D)/L + 2V_{in}R_iD/L$$

$$= 2V_{in}R_i/L \quad (13)$$

$$F_m = 1/(s_n + s_e)T_s = 1/T_s(2V_{in}R_i/L)$$

$$= L/(2V_{in}R_iT_s) \quad (14)$$

Note that the modulator gain, Fm, is in fact independent of duty cycle! This means the benefits of current-mode control are obtained while eliminating the output filter resonance and achieving near-perfect linearity as if pure voltage mode control were used. Since Fm is a constant, the model in Figure 3 can be applied for large-signal analysis as well.

The expression for V_{ext} is

$$V_{ext} = (V_{in}R_iT_s/L)D^2 \quad (15)$$

This function is plotted in Figure 8, and represents a parabola. For clocked on, comparator-off fixed frequency control, the parabola is easily synthesized by integrating a ramp that starts at the beginning of each clock cycle. Since the desired magnitude as given above is proportional to V_{in}, feedforward from the input DC rail (Figure 2) could be used when the design needs to accommodate a wide variation in input voltage, as is found in an off-line inverter.

Figure 7- PWM Comparator Inputs

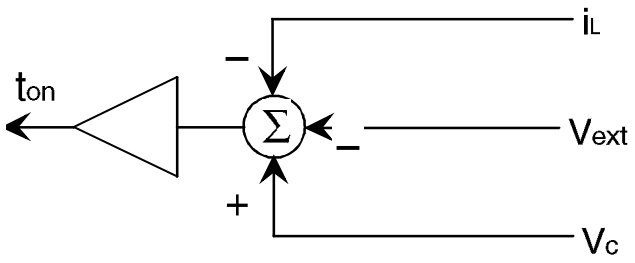
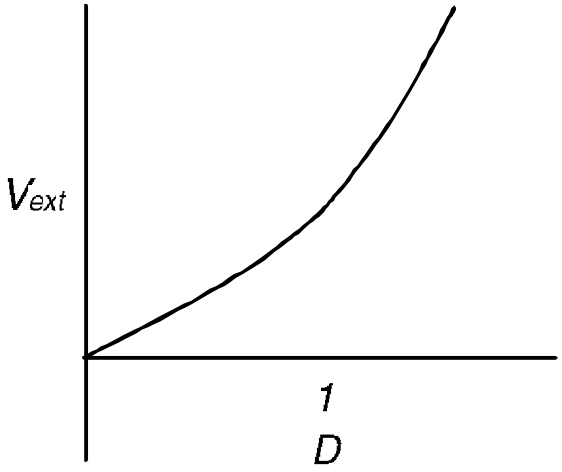


Figure 8- Vext Vs D



C. Subharmonic Stability

The sketch in Figure 9 graphically depicts the system response, $I_4 - I_3$, or ΔI_o, to a disturbance in the inductor current, $I_2 - I_1$, or ΔI_{in}. The following equations describe the system behavior, where $m_1 = s_n$ is the inductor current slope

during the on-time, and m_2 is the inductor current slope for the rest of the period T_s.

$V_{ext} = Kt^2$ describes the parabolic external ramp. (16)

$$I_1 - Kt_1^2 = m_1 t_1; I_2 - Kt_2^2 = m_1 t_2 \quad (17)$$

which yields

$$I_2 - I_1 = K\left(t_2^2 - t_1^2\right) + m_1(t_2 - t_1) \quad (18)$$

$$I_3 - Kt_1^2 = m_2(T_s - t_1); I_4 - Kt_2^2 = m_2(T_s - t_2) \quad (19)$$

which yields

$$I_4 - I_3 = K\left(t_2^2 - t_1^2\right) - m_2(t_2 - t_1) \quad (20)$$

The cycle to cycle attenuation, $-\Delta I_o/\Delta I_{in}$, is then

$$\frac{-(I_4 - I_3)}{(I_2 - I_1)} = \frac{K\left(t_2^2 - t_1^2\right) - m_2(t_2 - t_1)}{K\left(t_2^2 - t_1^2\right) + m_1(t_2 - t_1)} \quad (21)$$

It can be shown that the worst-case stability consideration is for $D = 1$, where $m_1 = 0$, and where $t_2 \cong t_1 = T_s$, which is the case analyzed below. Setting $m_1 = 0$ drops one term out of the denominator, and results in the following

$$-(I_4 - I_3)/(I_2 - I_1) = 1 - m_2(t_2 - t_1)/K\left(t_2^2 - t_1^2\right)$$

$$= 1 - m_2(t_2 - t_1)/K\left(t_2^2 - t_2 t_1 + t_2 t_1 - t_1^2\right)$$

$$= 1 - m_2(t_2 - t_1)/K(t_2(t_2 - t_1) + t_1(t_2 - t_1))$$

$$-(I_4 - I_3)/(I_2 - I_1) = 1 - m_2/K(t_2 + t_1) = 1 - m_2/K(2T_s) \quad (22)$$

It can be seen from this analysis that for the system to be marginally stable, the following relationship must apply:

$[1 - m_2/K(2T_s)] \le 1$; or $m_2/K(2T_s) \le 2$, for positive m_2.

or, $K \ge m_2/4T_s$. (23)

For the full-bridge inverter, m2 can be shown to be

$$m_2 = 2V_{in}R_i/L \quad (24)$$

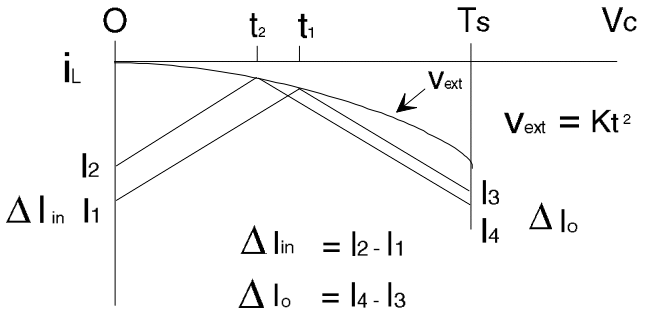
For stability, combining (23) and (24) gives

$$K \ge (2V_{in}R_i/L)/4T_s \quad (25)$$

which reduces to

$$K \ge V_{in}R_i T_s/2L \quad (26)$$

Figure 9- Subharmonic Stability



From (9), to achieve near-perfect linearity to guarantee low distortion, K should be

$$K = (V_{in}R_i T_s/L) \quad (27)$$

which is twice the minimum value of external ramp required for stability. Therefore stability is assured regardless of duty cycle!

Another method may be employed to determine relative stability. From [1] the control-to-output transfer function for current-mode control, a second-order continuous-time approximation to model the sampled-data nature of current-mode control is used. This small-signal analysis can be applied to our system by modeling the parabolic ramp as a linear ramp of equivalent slope at a particular operating point. The expression from [1] is given below for the equivalent Q of the second-order model.

Infinite Q would imply outright oscillation at certain duty-cycles when insufficient external ramp is added. High but finite values of Q result in peaking in the control-to-output transfer function, which can still lead to sub-harmonic oscillation at half the switching frequency when outer voltage-loop compensation is added.

Q is now determined given the values of parabolic ramp chosen earlier in this paper.

$$Q = 1/\pi(m_c D' - .5) \quad (28)$$

where

$$m_c = (1 + s_e/s_n) = (s_e + s_n)/s_n; \text{ and } D' = 1 - D \quad (29)$$

From (2) and (13)

$$m_c = (2V_{in}R_i/L)/2V_{in}R_i(1-D)/L = 1/(1-D) \quad (30)$$

Therefore

$$m_c D' = (1/(1-D))(1-D) = 1 \; ! \quad (31)$$

and

$$Q = 1/\pi(1-.5) = 2/\pi = .64 \quad (32)$$

The system is nearly critically damped for the values chosen.

II. MEASURED DATA

Distortion measurements of the system were taken with the linearity-corrected current-mode control loop in place, with no outer voltage loop control. Data is given for two different inversion frequencies for a full-bridge buck converter operating from a 400V rail, at 50KHz, with filter inductor and capacitor values of 500uH, and 2uF respectively.

Table 1 - Distortion vs Output Voltage

Output Voltage (rms)	Output Frequency (Hz)	Load resistor (ohms)	Distortion (THD) (%)
50	45	1000	0.21
100	45	1000	0.14
200	45	1000	0.14
50	500	1000	0.28
100	500	1000	0.27
200	500	1000	0.45

Total Harmonic Distortion (THD) was measured with an HP 8903B distortion analyzer, and is well below 1% for the region measured. Measurements of the control-to-output (voltage) transfer function without any voltage feedback also show no dependence on duty cycle, which corroborates these results.

Similiar measurements taken using a straight linear ramp instead of the linearity-corrected ramp resulted in total harmonic distortion (THD) between 4.2% to 4.7% for the same inversion frequency range of 50Hz to 500Hz.

III. CONCLUSIONS

A novel method for achieving low distortion performance from PWM AC inverters has been presented. The method has been verified both analytically and with measurements on a first prototype, and is easily implemented from signals already present in the system. The method is realized without compromise in sub-harmonic stability, and offers an order of magnitude improvement in open-loop distortion performance in comparison to standard methods.

ACKNOWLEDGMENTS

The author would like to thank Neil Yosinski, Ben Jansyn, Emery Salesky, and John Hyde for their contributions, comment, and review, as well as recognize the earlier creation and use of a parabolic ramp by Bob Peck and Mike Benes to stabilize PWM current-mode control systems for DC power supplies. My appreciation as well to Ray Ridley for creating an easily applied, accurate model for current-mode control. My upmost thanks to my administrative assistant Kazuko Ross for her initiative and dedication in preparing this manuscript.

REFERENCES

[1] A New, Continuous-Time Model for Current-Mode Control. Raymond B. Ridley. IEEE Transactions on Power Electronics, Vol 6, No 2, April 1991.

Dennis W. Gyma (M'92) attended Rutgers University in Piscataway, N.J. where he received his B.S. and M.S. degrees in Electrical Engineering in 1973 and 1975.

In 1975 he joined the New Jersey Division of Hewlett-Packard Company in Rockaway, N.J. as a project engineer. He has been responsible for generating new products and associated technology over his career in the areas of Power Supplies, Electronic Loads, AC Sources, and Uninterruptible Power Sources. He is now an R&D Program Manager for new product development. His technical interests include power electronics, power quality, circuit analysis, and embedded control.

Mr. Gyma was awarded a teaching fellowship by Rutgers University, and later served there as an adjunct professor in Power Electronics.